Multi-Scenario Analog and Mixed-Signal Circuit Routing with Agile Human Interaction (Extended Abstract)

Haoyi Zhang[1], Xiaohan Gao[2,1], Yibo Lin[1,3,4*], Runsheng Wang[1,3,4], Ru Huang[1,3,4]
[1]School of Integrated Circuits [2]School of Computer Science, Peking University
[3]Beijing Advanced Innovation Center for Integrated Circuits
[4]Institute of Electronic Design Automation, Peking University, Wuxi, China

2023 International Symposium of Electronics Design Automation (ISEDA) | 979-8-3503-0451-0/23/$31.00 ©2023 IEEE | DOI: 10.1109/ISEDA59274.2023.10218434

***Abstract*—The expanding markets of emerging applications create large demands for analog and mixed-signal (AMS) integrated circuits. This increasing demand calls for a shorter design cycle and time-to-market period. Routing is one of the most time-consuming and tedious steps in the design cycle. The generation of high-quality routing for AMS circuits still heavily relies on human efforts. Most previous studies only focus on the scenario of pure analog circuit blocks and cannot cover the versatile scenarios from real-world designs with both analog and digital circuit blocks. In this work, we propose an AMS routing engine for designs containing both analog and digital circuit blocks. Through the full cooperation of a multi-scenario routing engine and agile human interaction, the framework can generate high-quality routing solutions for AMS circuits.**

***Index Terms*—AMS circuit routing, multi-featured, agile human interaction**

I. Introduction

AMS layout design heavily relies on manual efforts. Routing is one of the most tedious steps in the layout design stage, where designers have to draw wire connections with their hands carefully. The AMS layout routing should consider not only analog scenarios but also customized digital scenarios. As Figure 1 indicates, to guarantee the performance and functionality, analog routing must consider versatile constraints such as EM [1], [2] & IR drop [3] constraints on power/ground nets and critical nets, symmetry constraint, sensitive area constraint, etc. While customized digital routing must support multiple features such as track routing, trunk routing, bus routing [4], etc. All of these constraints and features contribute to the better performance of the whole AMS layout automation system.

To automate AMS circuit routing, the literature has explored techniques to tackle various scenarios. However, most previous studies focus on a single feature, such as symmetry for analog layouts [5], [6], [7], EM and IR drop effects [8], [9], bus routing for digital circuits [4]. Although state-of-the-art AMS routing [10], [11] proposes a fancy detailed routing framework that considers multiple complex design rules, they still ignore a lot of customized digital scenarios in AMS circuit systems. Moreover, without human in the loop [12], all of these studies are fully automated tools that are difficult to obtain widespread acceptance in a short term.

In this paper, we propose a multi-scenario framework with agile human interaction for analog and mixed-signal integrated circuits. We summarize our main contributions as follows.

- We propose a multi-constraint routing framework for analog circuits which considers both geometric and electrical constraints, and our framework is compatible with manually placed layouts.
- We design a novel customized digital routing framework that supports arbitrary routing tracks as well as trunk routing and bus routing.

*Corresponding author: yibolin@pku.edu.cn

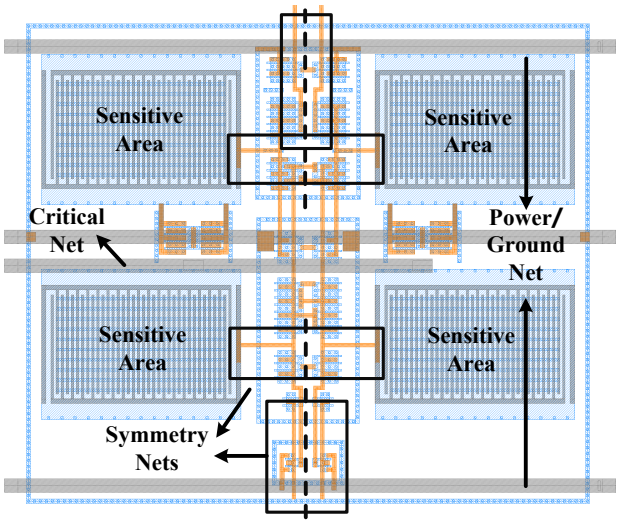

Fig. 1: A real-world layout example with multiple constraints considered.

- We develop an interactive routing algorithm to decrease the gap between the AMS layout generated by fully automated tools and the real-world AMS layout through human efforts.

The remainder of this paper is organized as follows. Section II details our implementation. Section III demonstrates the experimental results, and Section IV concludes the paper.

II. Methodology

In this section, we introduce the details of the proposed multi-scenario AMS routing framework.

A. Multi-constraint Analog Routing

The proposed analog routing considers both geometric constraints (e.g., design rules) and electrical constraints (e.g., EM and IR drop, symmetry, sensitive area, etc.). The framework takes circuit netlist as well as technology files including DRC rules, electromigration parameters, and metal layer parameters as input. Design configurations for IR drop (e.g., voltage margin and critical nets) and EM (e.g., operating temperature and critical nets) are also necessary. Before the major flow starts, a schematic simulation is conducted to generate the current information for the specified circuit netlist. The major flow consists of two phases: 1. Electrical constraints pre-processing; 2. Multi-constraint aware routing. Phase 1 involves Steiner tree-based wire sizing, symmetry type recognition, and sensitive area detection. The former determines wire width, the middle determines symmetry constraints and the latter generates routing obstacles, all of which will be used to guide the multi-constraint-aware routing in phase 2. Finally, a high-quality routing solution is generated.

Authorized licensed use limited to: Peking University. Downloaded on July 03,2025 at 06:21:14 UTC from IEEE Xplore. Restrictions apply.

B. Customized Digital Routing

Customized digital routing consists of multiple features such as track routing, trunk routing, and bus routing. The input of the customized digital routing is circuit netlist and feature configurations. According to the feature configurations given by designers, the customized digital routing tool generates the final layout net by net leveraging various routing features.

C. Interactive Routing Framework

Interactive routing can serve as a bridge connecting manual engineering efforts and automated layout generation tools. The input of the framework is an initial routing solution generated by automation tools. To formulate the editing process, a set of editing commands are determined. These editing commands include not only basic commands like removing and rerouting a single net, setting particular wire width, and adjusting the net's routing priority but also superior commands like adjusting the spacing between two designated wires and specifying rough routing topologies for nets. Designers are able to adjust the routing topology with these well-designed commands and get a legal routing solution without DRC violations instantly.

III. Result

The whole framework is implemented in C++ programming language. Our experiments platform is a Linux server with Intel Xeon Gold 6230 CPU @ 2.10GHz. We perform experiments on real-world AMS designs including an FIA and a SAR-ADC that have been taped out. We support routing on both automatically generated placement and manually-drawn placement, and finish routing within 20 seconds on each benchmark, which is much faster than manual process.

FIA is a kind of high-performance amplifier that is strict with the noise level. Compared with the manual layout, our framework obtains a 60% reduction of noise with a slightly lower gain. The analog part of a 12-bit SAR-ADC is the major routing object, while the digital part including CDAC (capacitor DAC) and control logic is excluded. As Table I depicts, our framework obtains a decent performance which is very close to the manual layout. Figure 2 shows the final layout of SAR-ADC.

TABLE I: Comparison on Benchmarks with Manual Placement.

Benchmark		Schematic	Manual	Our
FIA	Gain (dB)	24.55	**23.97**	**23.57**
	Noise (nV)	61.03	54.83	**21.44**
SAR-ADC	Delay (ns)	20.43	**21.37**	21.47
	SINAD (dB)	65.59	**65.74**	**65.70**
	ENOB (bit)	10.60	**10.63**	**10.62**
	Pcore (uW)	206.6	**231.6**	231.9
	FoM (fJ/conv)	5.321	**5.862**	**5.896**

1. Data bolded in black denotes the best, and data bolded in gray denotes the second best.

IV. Conclusions

In this paper, we propose a multi-scenario routing framework with agile human interaction. The framework is able to perform analog routing subject to various constraints like EM&IR drop and symmetry, customized digital routing with multiple features like trunk routing and bus routing, and interactive routing combined with human experience. Experimental results on real-world AMS designs in 65nm and 28nm technology nodes demonstrate the effectiveness of the framework and its compatibility with manual taped-out designs.

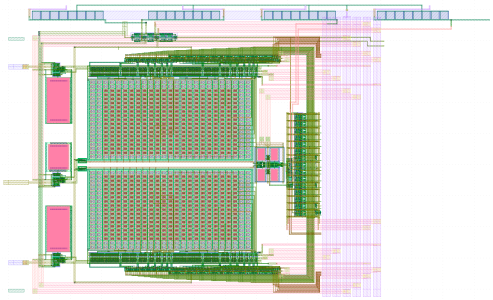

Fig. 2: SAR-ADC Final Layout

Acknowledgement

This work was supported in part by the National Science Foundation of China (Grant No. 62141404, 62125401).

References

[1] J. Black, "Electromigration—A brief survey and some recent results," *IEEE TED*, vol. 16, no. 4, pp. 338–347, 1969.

[2] J. Lienig and G. Jerke, "Electromigration-aware physical design of integrated circuits," in *Proc. VLSI Design*, 2005, pp. 77–82.

[3] Z. Chai, Y. Zhao, Y. Lin, W. Liu, R. Wang, and R. Huang, "Circuitnet: An open-source dataset for machine learning applications in electronic design automation (eda)," *SCIENCE CHINA Information Sciences*, vol. 65, no. 12, pp. 227 401–, 2022.

[4] C.-H. Hsu, S.-C. Hung, H. Chen, F.-K. Sun, and Y.-W. Chang, "A dag-based algorithm for obstacle-aware topology-matching on-track bus routing," *IEEE TCAD*, vol. 40, no. 3, pp. 533–546, 2021.

[5] U. Choudhury and A. Sangiovanni-Vincentelli, "Constraint-based channel routing for analog and mixed analog/digital circuits," *IEEE TCAD*, vol. 12, no. 4, pp. 497–510, 1993.

[6] R. Martins, N. Lourenço, and N. Horta, "Routing analog ics using a multi-objective multi-constraint evolutionary approach," *Analog Integrated Circuits and Signal Processing*, vol. 78, no. 1, pp. 123–135, Jan 2014.

[7] H.-C. Ou, H.-C. C. Chien, and Y.-W. Chang, "Nonuniform multilevel analog routing with matching constraints," *IEEE TCAD*, vol. 33, no. 12, pp. 1942–1954, 2014.

[8] R. Martins, N. Lourenço, A. Canelas, and N. Horta, "Electromigration-aware and ir-drop avoidance routing in analog multiport terminal structures," in *Proc. DATE*, 2014, pp. 1–6.

[9] M. Torabi and L. Zhang, "Electromigration- and Parasitic-Aware ILP-Based Analog Router," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 26, no. 10, pp. 1854–1867, 2018.

[10] H. Chen, K. Zhu, M. Liu, X. Tang, N. Sun, and D. Z. Pan, "Toward silicon-proven detailed routing for analog and mixed-signal circuits," in *Proc. ICCAD*, 2020, pp. 1–8.

[11] H. Zhang, X. Gao, H. Luo, J. Song, X. Tang, J. Liu, Y. Lin, R. Wang, and R. Huang, "Sageroute: Synergistic analog routing considering geometric and electrical constraints with manual design compatibility," in *Proc. DATE*, 2023, (To be published).

[12] X. Gao, H. Zhang, M. Liu, L. Shen, D. Pan, Y. Lin, R. Wang, and R. Huang, "Interactive analog layout editing with instant placement and routing legalization," *IEEE TCAD*, vol. PP, pp. 1–1, 01 2022.

Authorized licensed use limited to: Peking University. Downloaded on July 03,2025 at 06:21:14 UTC from IEEE Xplore. Restrictions apply.