张昊懿

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教育经历

北京大学 2022年09月 - 2027年06月
电子设计自动化与计算系统 博士 集成电路学院 北京
GPA: 3.66/4.00
荣誉奖励：**国家奖学金(2024)**、北京大学三好学生(2024)、
北京大学集成电路学院华为奖学金一等奖(2023)、北京大学优秀科研奖(2023)

北京航空航天大学 985 双一流 2018年09月 - 2022年06月
微电子科学与工程 本科 集成电路科学与工程学院 北京
GPA：3.75/4.00
荣誉奖项：**校级优秀毕业生、一等奖学金（前8%）**、校级三好学生

学术成果：论文发表

EDA--Analog CAD

1. HaoyiZhang* , XiaohanGao*, HaoyangLuo, etc. "SAGERoute: Synergistic Analog Routing Considering Geometric and Electrical Constraints with Manual Design Compatibility". **(DATE2023 Best Paper Award)**

2. HaoyiZhang, XiaohanGao, etc."SAGERoute 2.0: Hierarchical Analog and Mixed Signal Routing Considering Versatile Routing Scenarios" **(DATE2024)**

3. XiaohanGao*, **HaoyiZhang***, MingjieLiu, etc. Interactive Analog Layout Editing with Instant Placement and Routing Legalization, **(TCAD2022, co-first-author)**

4. HaoyiZhang, XiaohanGao, etc. "Multi-Scenario Analog and Mixed-Signal Circuit Routing with Agile Human Interaction" **(ISEDA2023)**

5. Xiaohan Gao, **HaoyiZhang**, etc. "Joint Placement Optimization for Hierarchical Analog/Mixed-Signal Circuits", **(ICCAD2024)**

6. Xiaohan Gao, **Haoyi Zhang**, etc. "Post-Layout Simulation Driven Analog Circuit Sizing" **(Science China 2023)**

7. YiboLin, XiaohanGao, **HaoyiZhang**, etc. "Intelligent and Interactive Analog Layout Design Automation", **(ICSICT2022)**

8. BingyangLiu, HaoningJiang, **HaoyiZhang**, etc. "GRAIN: A Design-Intent-Driven Interactive Analog Layout Migration Framework". **(ICCAD2025,submission)**

EDA--Design Space Exploration

9. **HaoyiZhang**, Jiahao Song, etc. "EasyACiM: An End-to-End Automated Analog CIl with Synthesizable Architecture and Agile Design Space Exploration"**(DAC2024)**

10. HaikangDiao*, **HaoyiZhang***,"SEGA-DCIM: Design Space Exploration-Guided Automatic Digital CIM Compiler with MultiplePrecision Support". **(DATE2025, co-first-author)**

EDA--AI4EDA

11. **HaoyiZhang**,ShizhaoSun, etc."AnalogXpert: Automating Analog Topology Synthesis by Incorporating Circuit Design Expertise into Large Language Models".**(ISEDA2025)**

12. **HaoyiZhang*,** JiechenHuang*, etc. "APEC-Route: Guiding Analog Routing with On-the-Fly Parasitic Extraction Based on Neural Capacitance Model". **(ICCAD25,submission)**

13. WeijianFan*, **HaoyiZhang***, etc. "AMSHBO: Multi-Stage Hierarchical Bayesian Optimization for Substructure-Aware High-Dimensional Analog Circuit Sizing". **(ICCAD25,submission)**

14. Bingyang Liu*, **HaoyiZhang***, etc. "LayoutCopilot: An LLM-powered Multi-agent

Collaborative Framework for Interactive Analog Layout Design", **(TCAD2024, co-first-author)**

15. Bingyang Liu, **HaoyiZhang**, etc. " LayoutCopilot: LLM-Empowered Analog Layout Design towards Enhanced Human-Machine Interaction"**(ISCAS2025)**

16. LeiChen,Yiqi Chen, Zhufei Chu, etc. **(Haoyi Zhang, co-author)**, "The dawn of ai-native eda: Promises and challenges of large circuit models" , **(Science China 2024)**

EDA--Standard Cell

17. KairongGuo, XiaohanGao, **HaoyiZhang** ,etc."Multi-Row Standard Cell Layout Synthesis with Enhanced Scalability". **(ISEDA2025)**

18. KairongGuo, XiaohanGao, HaoyiZhang , etc. "Exploring Better Intra-Cell Routability for Layout Synthesis of Multi-Row Standard Cells"**(ASP-DAC2025,Invited paper)**

Circuit Design

19. **HaoyiZhang**, Jiahao Song, etc. "A 266F2 Ultra Stable Differential NOR-Structured Physically Unclonable Function with < 6×10−9 Bit Error Rate Through Efficient Redundancy Strategy", **(TCAS-II 2024)**

20. A Calibration-Free 15-level/Cell eDRAM Computing-in-Memory Macro with 3T1C Current-Programmed Dynamic-Cascoded MLC achieving 233-to-304-TOPS/W 4b MAC, JiahaoSong, XiyuanTang, HaoyangLuo, **HaoyiZhang**, XinQiao. **(CICC 2023)**

21. A 4-bit Calibration-Free Computing-In-Memory Macro With 3T1C Current-Programed Dynamic-Cascode Multi-Level-Cell eDRAM. JiahaoSong, XiyuanTang, HaoyangLuo, **HaoyiZhang**, XinQiao. **(JSSC 2023)**

学术成果：专利授权

1. 一种多驱动能力的集成电路标准单元版图迁移的方法，申请日期：2023.02.06，公开号：CN115859899B，发明人：林亦波，高笑涵，**张昊懿**，王润声，黄如
2. 可处理电学和几何约束的模拟电路布线自动化方法及系统，申请日期：2022.11.15，公开号：CN115496030B，发明人：林亦波，高笑涵，**张昊懿**，王润声，黄如
3. 一种用于模拟电路版图布线的交互式编辑方法及工具，申请日期：2022.01.13，公开号：CN114510900B，发明人：林亦波，**张昊懿**，高笑涵，王润声，黄如

竞赛奖项

北京大学电子设计自动化系产业贡献奖(全系仅两人/年) 2023

EDA设计精英挑战赛华大九天企业特别奖 2021

EDA设计精英挑战赛全国二等奖 2021&2022

实习经历

字节跳动--筋斗云计划 2025年04月 - 至今

芯片物理设计 北京

1. 基于std cell生成的DTCO优化技术
2. 基于std cell生成的高质量IP block生成技术

微软亚洲研究院 2024年04月 - 2024年09月

研究岗 Machine Learning组 北京

研究使用大模型生成高质量模拟电路前端网表

华为技术有限公司（海思-图灵） 2023年07月 - 2023年09月

开发岗 上海

探索开发数字电路标准单元库点版图自动化设计方法

概伦电子科技（上海）有限公司 2022年07月 - 2023年01月

开发岗 北京

1. Analog Routing的协助落地，将SAGERoute中的基础特性嵌入概伦的nanospice仿真工具
2. Digital Routing for custom design 协助落地，开发能够适应custom design的routing工具

技能/证书及其他

- **技能：** C++、Python、Pytorch框架，Virtuoso，Innovus